

REMARKS

INTRODUCTION

In accordance with the foregoing, claims 1, 8, and 9 have been amended. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-10 are pending and under consideration. Reconsideration is respectfully requested.

ENTRY OF RESPONSE UNDER 37 C.F.R. §1.116

Applicants request entry of this Rule 116 Response and Request for Reconsideration because the amendment of claims 1, 8, and 9 should not entail any further search by the Examiner since the amendments only clarify the features of claims 1, 8, and 9. No new features are being added or no new issues are being raised. Further, the amendments do not significantly alter the scope of the claims and place the application at least into a better form for appeal.

The Manual of Patent Examining Procedures sets forth in §714.12 that "[a]ny amendment that would place the case either in condition for allowance or in better form for appeal may be entered." (Underlining added for emphasis) Moreover, §714.13 sets forth that "[t]he Proposed Amendment should be given sufficient consideration to determine whether the claims are in condition for allowance and/or whether the issues on appeal are simplified." The Manual of Patent Examining Procedures further articulates that the reason for any non-entry should be explained expressly in the Advisory Action.

REJECTION UNDER 35 U.S.C. §102(e)

In the Final Office Action at page 2, claims 1-10 were rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,457,126 to Nakamura, et al. This rejection is traversed and reconsideration is respectfully requested.

Independent claim 1 is directed to a storage device for maintaining information, which is accessed by a host device through a host interface, when the power is OFF and being capable of executing a test process based on test signals. In relevant part, independent claim 1 has been amended to recite "a decoding part decoding data read out by the memory stored at the memory location in response to the data reading instruction and determining whether the data is secret data or initial data," "a maintaining part maintaining information resulting from the

decoding in a volatile state," and "a cutting-off part cutting off the test signals input from the test terminal when the maintaining part maintains information indicating that secret data is stored at the memory location."

At page 3, the outstanding Office Action contends that Nakamura, et al. at col. 12, lines 5-12, and col. 13, lines 13-19 teaches "a decoding part decoding whether the data read out by the memory stored at the memory location in response to the data reading instruction is the secret data or the initial data." Col. 12, lines 5-12, of Nakamura, et al. teaches only that a controlling section 162 verifies the address of the decrypting program area by using an address counter. Applicants respectfully submit that this portion of Nakamura, et al. fails to teach a decoding part as recited in amended independent claim 1. Nakamura, et al. at col. 13, lines 13-19, states "In the above explanations, the controlling section 162 sequentially writes and reads data in the test mode. However, when the test mode is set, the storage device 10 may directly connect the external bus with an internal bus until the test mode is cancelled. Further, the test device 30 may have such a structure that it can directly access each memory." Again, Applicants respectfully submit that the cited art fails to teach or suggest a decoding part, as recited in amended independent claim 1.

At page 3, the outstanding Office Action contends that Nakamura, et al. at col. 12, lines 55-62 and col. 13, lines 20-25, teach "a cutting-off part cutting off the test signals input from the test terminal when the maintaining part maintains information indicating that the secret data is stored at the memory location." Applicants respectfully disagree. Nakamura, et al. at col. 12, lines 55-62, states

When all of the calculation results y_i and the entire expected values D_i coincide with each other, the controlling section 162 sends a coincidence detection signal to the test device 30 (Step S33). When any one of the calculation results y_i does not coincide with any of the entire expected values D_i , the controlling section 162 sends a mismatch detection signal to the test device 30 (Step 34), and the test operation ends by now.

Thus, according to Nakamura, et al., the test operation ends when the test operation detects an error, and not when secret data is stored at the memory location, as in the present invention.

Nakamura, et al. at col. 13, lines 20-25, states

In such a case, when the system key area T2 and the decrypting program area T3 are addressed, it is preferred that the second ROM 15 be set in a disable state, and that an address signal be masked in order not to accept (to prohibit) any external direct access. Particularly, as described in FIG. 6, an address signal at a high level may be decoded.

Nakamura, et al. at col. 7, lines 60-65, discloses that the second ROM 15 is a read-only

memory that has storage areas including a system key area T2, a decrypting program storage area T3, an expected value area T4, and a hash function area T5. According to Nakamura, et al., when the system key area T2 and the decrypting program area T3 are addressed, the test function is not affected. Rather, it is the second ROM 15 that is set in a disabled state to prohibit any external direct access. Thus, Applicants respectfully submit that Nakamura, et al. fails to teach or suggest "a cutting-off part cutting off the test signals input from the test terminal when the maintaining part maintains information indicating that secret data is stored at the memory location," as recited in amended independent claim 1.

Additionally, Applicants note that, in the test mode of Nakamura, et al., when hashed values are not matched to each other, data in the memory cannot be read out and protected. However, when the hashed values are successfully matched to each other, data in the memory can be read out. Thus, according to the teachings of Nakamura, et al., if a normal encryption key is stored in the memory, the data can be successfully read out.

In contrast, in the present invention, a test can be allowed only when a memory, such as flash memory (which is in a volatile state), including the encryption key is initialized. In the case of flash memory, for example, initialized data are all FF hex. Thus, when an encryption key is actually stored, the test cannot be allowed, thus providing improved security.

For at least these reasons, Applicants respectfully submit that Nakamura, et al. fails to teach or suggest all of the features of amended independent claim 1 and those claims depending directly or indirectly therefrom. Accordingly, Applicants respectfully submit that amended independent claim 1 and those claims depending therefrom are in condition for allowance.

Each of independent claims 8, 9, and 10 recite features similar to those of amended independent claim 1. Thus, Applicants respectfully submit that claims 8, 9, and 10 patentably distinguish over the prior art for reasons similar to those of amended independent claim 1 and, therefore, are in condition for allowance.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. And further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited. At a minimum, this Amendment should be entered at least for purposes of Appeal as it either clarifies and/or narrows the issues for consideration by the Board.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited and possibly concluded by the Examiner contacting the undersigned attorney for a telephone interview to discuss any such remaining issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 7 February 2008

By: Allison Olenginski
Allison Olenginski
Registration No. 55,509

1201 New York Ave, N.W., Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501